

CMOS Digital Integrated Circuit Silicon Monolithic

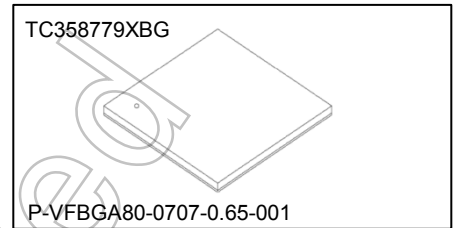
# TC358779XBG

Mobile Peripheral Devices

## Overview

The HDMI-RX to MIPI DSI-TX is a bridge device that converts HDMI® stream to MIPI® DSI while providing de-interlacing and auto-scaling features.

TC358779XBG share the same 80-pin package as that of TC358749XBG.



Weight: 77mg (Typ.)

## Features

- **HDMI-RX Interface**
  - ✧ HDMI® 1.4b
    - Video Formats Support (Up to 1080P @60fps)
      - RGB, YCbCr444: 24-bpp @60fps
      - YCbCr422 24-bpp @60fps
    - Audio Supports
      - Internal Audio PLL to track N/CTS value transmitted by the ACR packet.
    - 3D Support
    - HDCP1.3 Support (optional)
    - EDID Support
      - Release A, Revision 1 (Feb 9, 2000)
      - First 128 byte (EDID 1.3 structure)
      - First E-EDID Extension: 128 bytes of CEA Extension version 3 (specified in CEA-861-D)
      - Embedded 1 K-byte SRAM (EDID\_SRAM)
    - Maximum HDMI® clock speed: 165 MHz
  - ✧ Does not support Audio Return Path and HDMI® Ethernet Channels
- **DSI TX Interface**
  - ✧ MIPI DSI compliant (Version 1.1 22 November 2011)
  - ✧ Supports up to 4 data lanes @1Gbps/lane
  - ✧ Supports video data formats
    - RGB888 or RGB666
- **I<sup>2</sup>C Slave Interface**
  - ✧ Support for normal (100 kHz), fast mode (400 kHz) and ultra-fast mode (2 MHz)
  - ✧ Configure all TC358779XBG internal registers
  - ✧ Support 2 I<sup>2</sup>C Slave Addresses (7'h0F & 7'h1F) selected through boot-strap pin (INT)
- **Audio Output Interface**

Any of the three audio interfaces are available: I2S, TDM or IEC60958 (pins are multiplexed)

  - ✧ **I2S Audio Interface**
    - Up to 4 data lanes for 8-channel data
    - Support Master Clock mode only
  - Support 16, 18, 20 or 24-bit data (depend on HDMI® input stream)
  - Support Left or Right-justify with MSB first
  - Support 32 bit-wide time-slot only
  - Output Audio Over Sampling clock (256fs)
  - Support IEC 60958 & 61937 formats (depending upon HDMI® input stream) over I2S
  - Supports HBR audio stream split across 4 I2S lines if bandwidth higher than 12 MHz
  - ✧ **TDM (Time Division Multiplexed) Audio Interface**
    - Fixed to 8 channels
    - Support Master Clock mode only
    - Support 16, 18, 20 or 24-bit PCM audio data word (depend on HDMI® input stream)
    - Support 32 bit-wide time slot only
    - Output Audio OverSampling clock (256fs)
  - ✧ **Digital Audio Interface**
    - Supports 2 channels (any 2 of the total 8) (depend on HDMI® input stream)
    - Support IEC 60958 & 61937 formats (depending upon HDMI® input stream)
- **Video Processing**
  - ✧ Input formats accepted:
    - RGB or YCbCr422
    - Interlaced or Progressive
    - 2D or 3D
  - Limited to 165 MHz PClk, 640×480, 720×480, 720×576, 1280×720 or 1920×1080 are expected when scalar is used
  - ✧ Output formats supported:
    - RGB888 or RGB666
    - Interlaced (in case of no video processing) or Progressive
    - 2D or 3D
    - Limited by 4Gbps D-PHY bandwidth, 720×480, 1280×720 or 1920×1080 are expected when scalar is invoked

## ✧ Scaling:

- Hardware performs scaling automatically based on input and output frame size
  - HDMI Rx received input frame size and Panel size programmed in registers
  - Can be overwritten by Software if necessary
- Horizontal Scaling factors supported:
  - 3-to-2, 1-to-2, 3-to-4, 3-to-8, 9-to-4 and 9-to-16
  - 2-to-3 and 1-to-3
- Vertical Scaling factors supported:
  - 1-to-2, 3-to-2 and 3-to-4
  - 2-to-1 and 3-to-1
  - 2-to-3 and 4-to-9
  - 4-to-5 and 8-to-15
- Special handling of 3D formats FP, SBS & T&B to avoid boundary artifacts.

## ✧ Color Space Conversion

- RGB ⇔ YCbCr
- Two sets of coefficients provided – 1 set for each direction
- Both color space convertors can be enabled/disabled independent of each other.

## ● InfraRed (IR)

- ✧ Support NEC InfraRed protocol.

## ● System

- ✧ Internal core has two power domains (VDDC1 and VDDC2)
  - VDDC1 is “always-on” power domain
  - VDDC2 can be shut-off during deep sleep mode

## ● Power supply inputs

- ✧ Core and MIPI D-PHY: 1.2 V
- ✧ I/O: 1.8 V – 3.3 V
- ✧ HDMI@: 3.3 V
- ✧ VPLL: 1.2 V

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**REFERENCES**

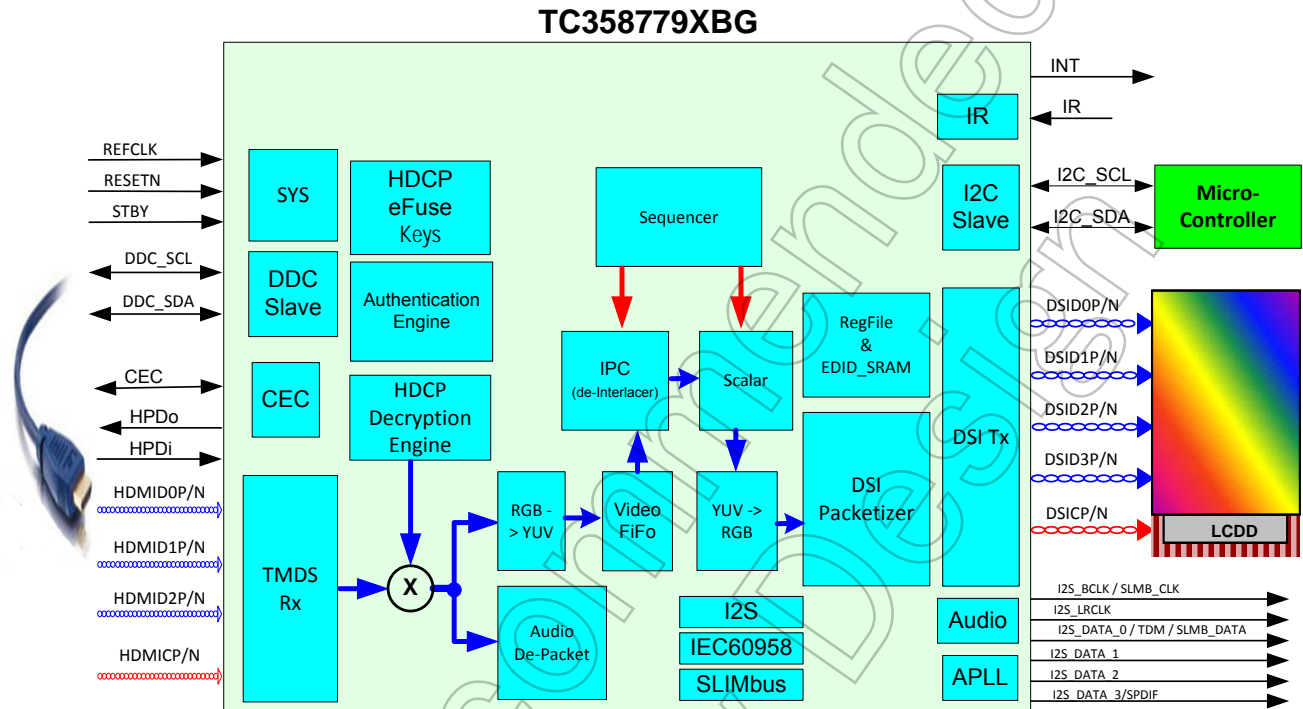
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2. MIPI DSI, “MIPI Alliance Specification for Display Serial Interface (DSI) Version 1.1 Revision 22 Nov 2011”
3. HDMI®, “High-Definition Multimedia Interface Specification Version 1.4b March 4, 2010”
4. I<sup>2</sup>C bus specification, version 2.1, January 2000, Philips Semiconductor
5. IEC 60958, Digital Audio Interface, First Edition, 1999
6. IEC 61937, Digital audio – Interface for non-linear PCM encoded audio bit streams
7. MIPI SlimBus, “MIPI Alliance Specification for Serial Low-power Inter-chip Media Bus (SLIMbus) Version 1.01.01 – 14 July 2008”

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# 1. Overview

The HDMI-RX to MIPI DSI-TX is a bridge device that converts HDMI® stream to MIPI® DSI while providing de-interlacing and auto-scaling features.

System Overview block diagrams are shown below. TC358779 XBG share the same 80-pin package as that of TC358749XBG.



**Figure 1.1 TC358779XBG System Overview**

## 2. Features

Below are the main features supported by TC358779XBG.

- HDMI-RX Interface
  - ◇ HDMI® 1.4b
    - Video Formats Support (Up to 1080P @60fps)
      - RGB, YCbCr444: 24-bpp @60fps
      - YCbCr422 24-bpp @60fps
    - Audio Supports
      - Internal Audio PLL to track N/CTS value transmitted by the ACR packet.
    - 3D Support
    - HDCP1.3 Support (optional)
    - EDID Support
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      - First 128 byte (EDID 1.3 structure)
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      - Embedded 1K-byte SRAM (EDID\_SRAM)
    - Maximum HDMI® clock speed: 165 MHz
  - ◇ Does not support Audio Return Path and HDMI® Ethernet Channels
- DSI TX Interface
  - ◇ MIPI DSI compliant (Version 1.1 22 November 2011)
  - ◇ Supports up to 4 data lanes @1Gbps/lane
  - ◇ Supports video data formats
    - RGB888 or RGB666
- I<sup>2</sup>C Slave Interface
  - ◇ Support for normal (100 kHz), fast mode (400 kHz) and ultra-fast mode (2 MHz)
  - ◇ Configure all TC358779XBG internal registers
  - ◇ Support 2 I<sup>2</sup>C Slave Addresses (7'h0F & 7'h1F) selected through boot-strap pin (INT)
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Any of the three audio interfaces are available: I2S, TDM or IEC60958 (pins are multiplexed)

  - ◇ I2S Audio Interface
    - Up to 4 data lanes for 8-channel data
    - Support Master Clock mode only
    - Support 16, 18, 20 or 24-bit data (depend on HDMI® input stream)
    - Support Left or Right-justify with MSB first
    - Support 32 bit-wide time-slot only
    - Output Audio Over Sampling clock (256fs)
    - Support IEC 60958 & 61937 formats (depending upon HDMI® input stream) over I2S
    - Supports HBR audio stream split across 4 I2S lines if bandwidth higher than 12 MHz

- ◇ TDM (Time Division Multiplexed) Audio Interface
  - Fixed to 8 channels
  - Support Master Clock mode only
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  - Output Audio OverSampling clock (256fs)
- ◇ Digital Audio Interface
  - Supports 2 channels (any 2 of the total 8) (depend on HDMI® input stream)
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  - ◇ Input formats accepted:
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    - Interlaced or Progressive
    - 2D or 3D
    - Limited to 165 MHz PClk, 640×480, 720×480, 720×576, 1280×720 or 1920×1080 are expected when scalar is used
  - ◇ Output formats supported:
    - RGB888 or RGB666
    - Interlaced (in case of no video processing) or Progressive
    - 2D or 3D
    - Limited by 4Gbps D-PHY bandwidth, 720×480, 1280×720 or 1920×1080 are expected when scalar is invoked
  - ◇ Scaling:
    - Hardware performs scaling automatically based on input and output frame size
      - HDMI Rx received input frame size and Panel size programmed in registers
      - Can be overwritten by Software if necessary
    - Horizontal Scaling factors supported:
      - 3-to-2, 1-to-2, 3-to-4, 3-to-8, 9-to-4 and 9-to-16
      - 2-to-3 and 1-to-3
    - Vertical Scaling factors supported:
      - 1-to-2, 3-to-2 and 3-to-4
      - 2-to-1 and 3-to-1
      - 2-to-3 and 4-to-9
      - 4-to-5 and 8-to-15
    - Special handling of 3D formats FP, SBS & T&B to avoid boundary artifacts.
  - ◇ Color Space Conversion
    - RGB ⇔ YCbCr
    - Two sets of coefficients provided – 1 set for each direction
    - Both color space converters can be enabled/disabled independent of each other.



- InfraRed (IR)
  - ✧ Support NEC InfraRed protocol.
  
- System
  - ✧ Internal core has two power domains (VDDC1 and VDDC2)
    - VDDC1 is “always-on” power domain
    - VDDC2 can be shut-off during deep sleep mode
  
- Power supply inputs
  - ✧ Core and MIPI D-PHY: 1.2 V
  - ✧ I/O: 1.8 V – 3.3 V
  - ✧ HDMI®: 3.3 V
  - ✧ VPLL: 1.2 V
  - ✧ Power Consumption during typical operations at room temperature

**Table 2-1 Power Consumption**

		VDDC1	VDDC2	VDDIO1	VDDIO2	VDDMIPI	AVDD33	AVDD12	AVDDPLL	Total Power (mW)
		1.2V	1.2V	3.3V	1.8V	1.2V	3.3V	1.2V	1.2V	
<b>1080P @ 60fps</b>	Current (mA)	61.13		0.80	0.89	20.50	72.80	67.82	0.01	423.83
	Power (mW)	73.36		2.64	1.60	24.60	240.24	81.38	0.01	
<b>720p → 1080p @ 30fps</b>	Current (mA)	170.40		0.80	0.89	20.02	72.66	56.67	1.12	541.87
	Power (mW)	204.48		2.64	1.60	24.02	239.78	68.00	1.34	

Note:

- TC358779XBG does not perform YCbCr ⇔ YUV conversion. In this document YCbCr, HDMI® terminology, is used to indicate video color space.

### 3. External Pins

Following table gives the signals of TC358779XBG and their function.

**Table 3-1 TC358779XBG Pin Name**

Group	Pin Name	I/O	Init (O)	Type	Function	Note
System: Reset & Clock (5)	RESETN	I	-	Sch	System reset input, active low	1.8V -3.3V
	REFCLK	I	-	N	Reference clock input (27/26MHz or 42MHz range)	1.8V -3.3V
	TEST	I	-	N	0: Normal mode 1: Test mode	1.8V -3.3V
	STBY	I	-	N	Standby pin, active low	1.8V -3.3V
	INT	O	L	N	Interrupt Output signal – active high (Level) I <sup>2</sup> C Slv_Addr_Sel at boot-strap	1.8V -3.3V
DSI TX (10)	MIPI_CP	O	H	MIPI-PHY	MIPI-DSI clock positive	1.2 V
	MIPI_CN	O	H	MIPI-PHY	MIPI-DSI clock negative	1.2 V
	MIPI_D0P	O	H	MIPI-PHY	MIPI-DSI Data 0 positive	1.2 V
	MIPI_D0N	O	H	MIPI-PHY	MIPI-DSI Data 0 negative	1.2 V
	MIPI_D1P	O	H	MIPI-PHY	MIPI-DSI Data 1 positive	1.2 V
	MIPI_D1N	O	H	MIPI-PHY	MIPI-DSI Data 1 negative	1.2 V
	MIPI_D2P	O	H	MIPI-PHY	MIPI-DSI Data 2 positive	1.2 V
	MIPI_D2N	O	H	MIPI-PHY	MIPI-DSI Data 2 negative	1.2 V
	MIPI_D3P	O	H	MIPI-PHY	MIPI-DSI Data 3 positive	1.2 V
MIPI_D3N	O	H	MIPI-PHY	MIPI-DSI Data 3 negative	1.2 V	
HDMI RX (8)	HDMICP	I	-	HDMI-PHY	HDMI Clock channel positive	3.3V
	HDMICN	I	-	HDMI-PHY	HDMI Clock channel negative	3.3V
	HDMID0P	I	-	HDMI-PHY	HDMI Data 0 channel positive	3.3V
	HDMID0N	I	-	HDMI-PHY	HDMI Data 0 channel negative	3.3V
	HDMID1P	I	-	HDMI-PHY	HDMI Data 1 channel positive	3.3V
	HDMID1N	I	-	HDMI-PHY	HDMI Data 1 channel negative	3.3V
	HDMID2P	I	-	HDMI-PHY	HDMI Data 2 channel positive	3.3V
HDMID2N	I	-	HDMI-PHY	HDMI Data 2 channel negative	3.3V	
DDC (2)	DDC_SCL	OD	-	FS-SOD	DDC Slave Clock	3.3V <sup>(Note1)</sup>
	DDC_SDA	OD	-	FS-SOD	DDC Slave data	3.3V <sup>(Note1)</sup>
CEC	CEC	OD	-	FS-SOD	CEC signal	3.3V
HPD (2)	HPDI	I	-	N	Hot Plug Detect Input	3.3V <sup>(Note1)</sup>
	HPDO	O	L	N	Hot Plug Detect Output	3.3V
Audio (7)	A_SCK	O	L	N	I2S/TDM Bit/S�IMbus Clock signal	1.8V -3.3V
	A_WFS	O	L	N	I2S Word Clock or TDM Frame Sync signal	1.8V -3.3V
	A_SD[0]	O	L	N	I2S (ch. 0,1)/TDM/S�IMbus data signal	1.8V -3.3V
	A_SD[2:1]	O	LL	N	I2S (ch. 2,3,4,5) data signal	1.8V -3.3V
	A_SD[3]	O	L	N	I2S (ch. 6,7) data/SPDIF signal	1.8V -3.3V
A_OSCK	O	L	N	Audio Over Sampling Clock	1.8V -3.3V	
IR	IR	I	-	Sch	InfraRed signal	1.8V -3.3V
I2C (2)	I2C_SCL	OD	-	FS-SOD	I <sup>2</sup> C serial clock	1.8V -3.3V
	I2C_SDA	OD	-	FS-SOD	I <sup>2</sup> C serial data	1.8V -3.3V
APLL (4)	BIASDA	O	L	-	BIAS signal	-
	DAOUT	O	H	-	Audio PLL clock Reference Output clock	-
	PCKIN	I	-	-	Audio PLL Reference Input clock	-
	PFIL	O	L	-	Audio PLL Low Pass Filter signal	-
POWER (11)	VDDC1	-	-	-	VDD for Internal Core (always ON) (1)	1.2V
	VDDC2	-	-	-	VDD for Internal Core (can be powered down) (2)	1.2V
	VDDIO1	-	-	-	VDDIO1 IO power supply (1)	3.3V
	VDDIO2	-	-	-	VDDIO2 IO power supply (1)	1.8V - 3.3V
	VDD_MIPI	-	-	-	VDD for the MIPI DSI (1)	1.2V
	VDD_PLL11	-	-	-	VDD for PLL11 (1)	1.2V
	AVDD12	-	-	-	HDMI PHY 1.2V power supply (2)	1.2V
AVDD33	-	-	-	HDMI PHY & APLL 3.3V power supply (2)	3.3V	
Ground (25)	VSS	-	-	-	Ground (25)	-
Misc	REXT <sup>(Note2)</sup>	-	-	-	External Reference Resistor	-
	VPGM <sup>(Note3)</sup>	-	-	-	eFuse program power supply	-

Total 80 pins

Note1: These IO are 5 V tolerant.

Note2: Please connect REXT to AVDD33 with a 2 k $\Omega$  resistor ( $\pm 1\%$ )

Note3: Please tie to ground

**Buffer Type Abbreviation:**

N: Normal IO  
FS-SOD: Failed Safe Pseudo open-drain output, Schmitt input  
Sch: Schmitt input buffer  
MIPI-PHY: front-end analog IO for DSI  
HDMI-PHY: front-end analog IO for HDMI®

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### 3.1. Pin Summary

**Table 3-2 Pin Count Summary – TC358779XBG**

Group Name	Pin Count
SYSTEM	5
DSI TX	11
HDMI RX	13
DDC	2
CEC	1
Audio	7
I2C	2
IR	1
HPD	2
APLL	4
POWER	7
GROUND	25
<b>TOTAL</b>	<b>80</b>

### 3.2. Pin Layout

#### Top View (through the die)

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
AVDD12	REXT	VDDC2	BIASDA	DAOUT	PFIL	VSS	VDD_PLL11	MIPI_D3N	MIPI_D3P
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10
AVDD33	VSS	VSS	VSS	VSS	VSS	PCKIN	VSS	MIPI_D2N	MIPI_D2P
C1	C2	C3	C4	C5	C6	C7	C8	C9	C10
HDMICP	HDMICN							MIPI_CN	MIPI_CP
D1	D2	D3	D4	D5	D6	D7	D8	D9	D10
HDMID0P	HDMID0N		VSS	VSS	VSS	VSS		VSS	VDD_MIPI
E1	E2	E3	E4	E5	E6	E7	E8	E9	E10
HDMID1P	HDMID1N		VSS	VSS	VSS	VSS		MIPI_D1N	MIPI_D1P
F1	F2	F3	F4	F5	F6	F7	F8	F9	F10
HDMID2P	HDMID2N		VSS	VSS	VSS	VSS		MIPI_D0N	MIPI_D0P
G1	G2	G3	G4	G5	G6	G7	G8	G9	G10
AVDD33	VSS		VPGM	TEST	VSS	VSS		VSS	A_OSK
H1	H2	H3	H4	H5	H6	H7	H8	H9	H10
AVDD12	CEC							A_SD_0	A_WFS
J1	J2	J3	J4	J5	J6	J7	J8	J9	J10
DDC_SCL	DDC_SDA	HPDO	INT	I2C_SCL	IR	REFCLK	VSS	A_SCK	A_SD_1
K1	K2	K3	K4	K5	K6	K7	K8	K9	K10
VDDC1	VDDIO1	HPDI	STBY	I2C_SDA	RESETN	VDDIO2	A_SD_3	A_SD_2	VDDC2

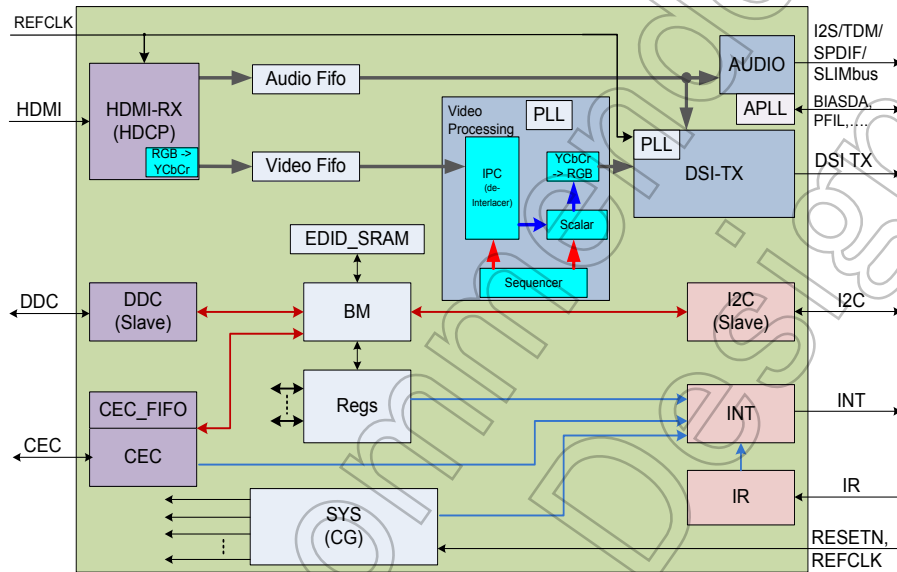
**Figure 3.1 TC358779XBG 80-Pin Layout Package (Top View)**

### 4. Major Functional Blocks

TC358779XBG consists of the following major blocks: HDMI-RX, DSI Tx, RGB2YCbCr & YCbCr2RGB color convertors, De-Interlacer, Scalar, DDC, CEC, I2S, TDM, IEC60958, INT and I<sup>2</sup>C i/f.

DDC, CEC and I<sup>2</sup>C slave controller are always enabled which are required for configuring the TC358779XBG chip and to wake up TC358779XBG chip.

The following sections describe each block in detail. In addition, there is a section that describes Clock generation block.

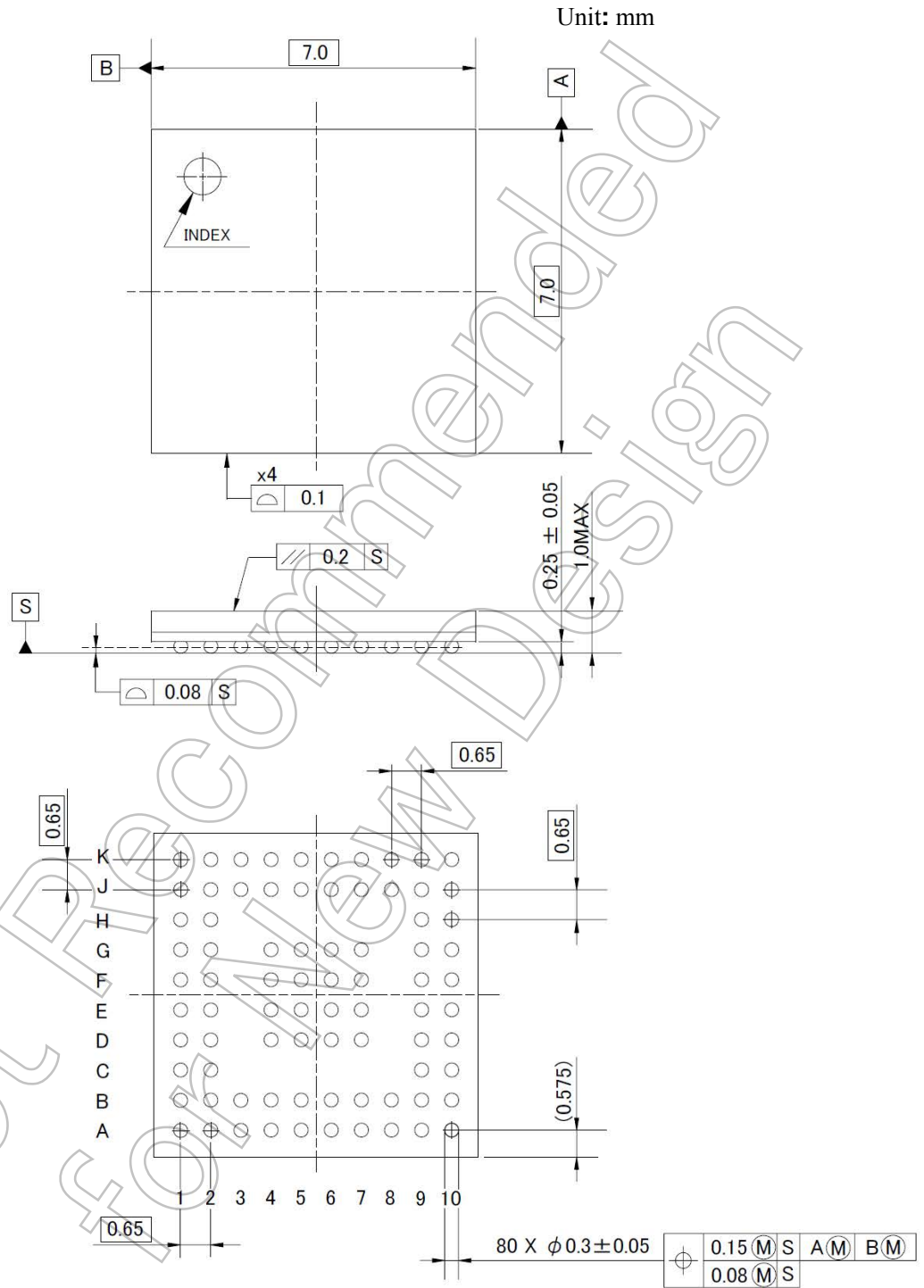


**Figure 4.1 Block Diagram of TC358779XBG**

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**5. Package**

TC358779XBG Package (80-pin, P-VFBGA80-0707-0.65-001)



Weight: 77mg (Typ.)

**Table 5-1 Mechanical Dimension for TC358779XBG**

Dimension	Min	Typ.	Max
Solder ball pitch	-	0.65 mm	-
Package dimension	-	7.0 × 7.0 mm <sup>2</sup>	-
Package height	-	-	1.0 mm

## 6. Electrical Characteristics

### 6.1. Absolute Maximum Ratings

VSS = 0 V reference

Parameter	Symbol	Rating	Unit
Supply voltage (1.8 V - Digital IO)	VDDIO	-0.3 to +3.9	V
Supply voltage (1.2 V - Digital Core)	VDDC	-0.3 to +1.8	V
Supply voltage (1.2 V - MIPI DSI PHY)	VDD_MIPI	-0.3 to +1.8	V
Supply voltage (3.3 V - HDMIRX PHY)	AVDD33	-0.3 to +3.9	V
Supply voltage (1.2 V - HDMIRX PHY)	AVDD12	-0.3 to +1.8	V
Input voltage (DSI IO)	V <sub>IN_DSI</sub>	-0.3 to VDD_MIPI+0.3	V
Output voltage (DSI IO)	V <sub>OUT_DSI</sub>	-0.3 to VDD_MIPI+0.3	V
Input voltage (Digital IO)	V <sub>IN_IO</sub>	-0.3 to VDDIO+0.3	V
Output voltage (Digital IO)	V <sub>OUT_IO</sub>	-0.3 to VDDIO+0.3	V
Junction temperature	T <sub>j</sub>	125	°C
Storage temperature	T <sub>stg</sub>	-40 to +125	°C

### 6.2. Recommended Operating Condition

VSS = 0 V reference

Parameter	Symbol	Min	Typ.	Max	Unit
Supply voltage (1.8/3.3 V - Digital IO)	VDDIO2	1.65	1.8	3.6	V
Supply voltage (3.3 V - HDMI Digital IO)	VDDIO1	3.0	3.3	3.6	V
Supply voltage (1.2 V - Digital Core)	VDDC	1.1	1.2	1.3	V
Supply voltage (3.3 V - HDMIRX PHY)	AVDD33	3.135	3.3	3.465	V
Supply voltage (1.2 V - HDMIRX PHY)	AVDD12	1.15	1.2	1.25	V
Supply voltage (1.2 V - MIPI DSI PHY)	VDD_MIPI	1.1	1.2	1.3	V
Operating temperature (ambient temperature with voltage applied)	T <sub>a</sub>	-30	+25	+70	°C
Supply Noise Voltage	V <sub>SN</sub>	-	-	100	mV <sub>pp</sub>

**6.3. DC Electrical Specification**

Parameter	Symbol	Min	Typ.	Max	Unit
Input voltage, High level input <sup>Note1</sup>	V <sub>IH</sub>	0.7 x VDDIO	-	VDDIO	V
Input voltage, Low level input <sup>Note1</sup>	V <sub>IL</sub>	0	-	0.3 x VDDIO	V
Input voltage High level CMOS Schmitt Trigger <sup>Note1,2</sup>	V <sub>IHS</sub>	0.7 x VDDIO	-	VDDIO	V
Input voltage Low level CMOS Schmitt Trigger <sup>Note1,2</sup>	V <sub>ILS</sub>	0	-	0.3 x VDDIO	V
Output voltage High level <sup>Note1, Note2</sup>	V <sub>OH</sub>	0.8 x VDDIO	-	VDDIO	V
Output voltage Low level <sup>Note1, Note2</sup>	V <sub>OL</sub>	0	-	0.2 x VDDIO	V
Input leak current, High level (Condition: V <sub>IN</sub> = +VDDIO, VDDIO = 3.6 V)	I <sub>ILH1</sub> <sup>(Note4)</sup>	-10	-	10	μA
Input leak current, Low level (Condition: V <sub>IN</sub> = 0 V, VDDIO = 3.6 V)	I <sub>ILL1</sub> <sup>(Note5)</sup>	-10	-	10	μA

Note1: Each power source is operating within recommended operation condition.

Note2: Current output value is specified to each IO buffer individually. Output voltage changes with output current value.

Note4: Normal pin or Pull-up IO pin applied VDDIO supply voltage to Vin (input voltage)

Note5: Normal pin applied VSS (0V) to Vin (input voltage)

Not Recommended for New Design



## 7. Revision History

Table 7-1 Revision History

Revision	Date	Description
0.75	2014-04-10	Newly released
0.821	2015-12-18	Typo Init(O) DAOUT pin in External Pins
0.822	2016-04-01	•Package's weight is rounding up digits after the decimal point to form an integer.
0.823	2016-09-01	1. Typo Correction on DSI-TX (10) on Table 3.1 2. Unified "Phy" to "PHY".
1.0	2017-10-17	Added comment to HDCP. Modified Table 3.2. Changed header, footer and the last page. Changed corporate name.
1.1	2017-11-13	Modified values in Table 2-1.

Not Recommended for New Design

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